

# Two 4 Layer PCB Stackups With 50 Ohms Impedance

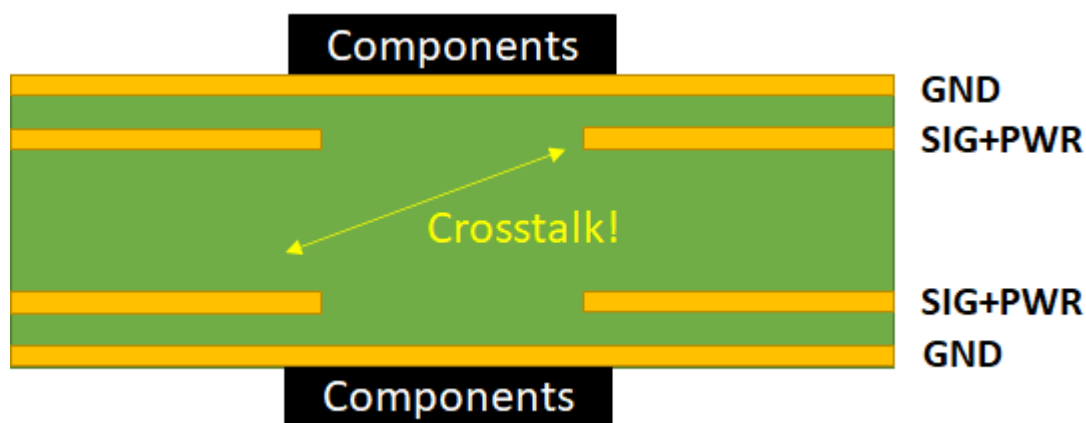
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New designers who graduate from a 2-layer board into a 4-layer board are probably ready to start working with power and ground planes, and there is a standard stackup most fabricators will give you to help build out your design. The basic stackup you'll often see recommended is a SIG/GND/PWR/SIG type stackup, where the internal layers are planes or large polygons. For many types of designs, this is just fine as long as you don't make some simple layout and routing mistakes.

If you need to do something more advanced, like placement and routing of high speed components on both sides of the board, you'll need to use an alternative stackup. The typical routing mistake that results in the basic 4-layer stackup involves routing high-speed signals between the surface layers without providing a clear return path, resulting in lots of radiated EMI from the board. Instead, you should use one of these alternative 4-layer stackups to create your PCB stackup and layout.

## Stackup #1: GND/SIG+PWR/SIG+PWR/GND

This stackup uses ground on the outer layers to provide high shielding against external EMI. It can also provide a nice easy path for ESD back to GND and eventually to the device chassis or earth without needing to follow a path through a via to an internal layer. This type of design, with ground on the outer layers and low impedance connections to GND directly with traces, is definitely the safest design from an EMI and ESD standpoint. It also nicely scales to higher layer counts if needed.



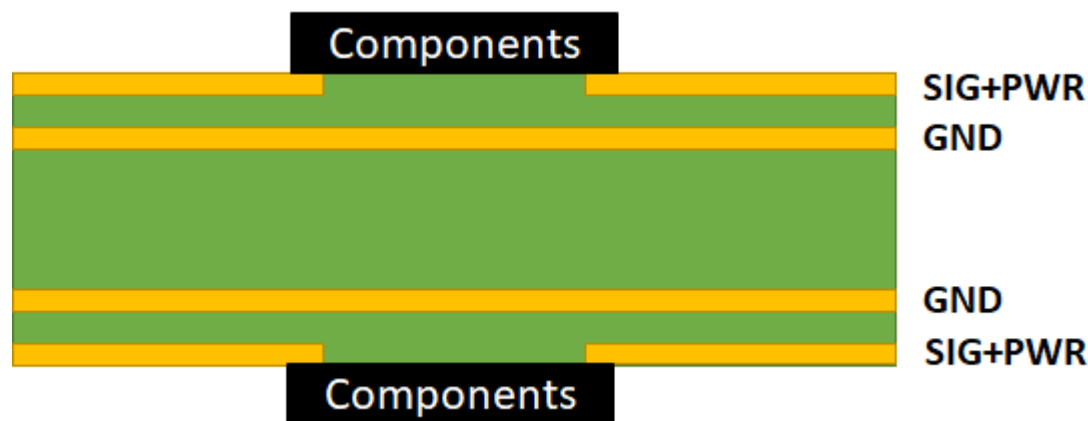
*This stackup provides high shielding against external noise, but it does little to suppress internal noise (crosstalk) between high speed signals on different layers.*

The potential problem with this stackup is crosstalk between signals on different layers. Normally, the thick core in the board will be ~40 mils or so, but this is not necessarily enough distance to guarantee traces won't receive crosstalk, especially at high speeds. The best way to prevent inductive crosstalk is with orthogonal routing on different layers. In addition, don't use this with excessively high speed signals or high frequencies, otherwise you might see capacitive crosstalk between signal layers (much more of a problem at high power GHz frequencies).

To eliminate the crosstalk problem, consider inverting this stackup as shown below.

## Stackup #2: SIG+PWR/GND/GND/SIG+PWR

For me, this stackup is preferable, particularly for any board where high speed signals need to transition between the two surface layers of the board. This stackup is just an inversion of the previous stackup. However, its function is different and it is not necessarily meant to provide high isolation from external noise sources. Instead, it is a better option for systems that require high speed components and routing on both sides of the board. It is also easy to design this [4-layer stackup for 50 Ohm controlled impedance](#). Finally, make sure to connect the GND planes with a via nearby wherever a signal transition is made.



*In the SIG+PWR/GND/GND/SIG+PWR stackup, it's possible that the digital return current in the PWR plane follows a very large loop back to ground. One path is through the nearest decap, but this does not eliminate low-frequency EMI.*

The tradeoff with this stackup is lower shielding for signals on the outer layer. Signals on each side of the board are shielded from each other, but not from external radiation sources. This stackup has another advantage in that you can route directly into components without needing to cut up the ground plane. Overall, these advantages in this stackup and the previous stackup are ideal for high speed designs with routing on both surfaces compared to the standard SIG/PWR/GND/SIG stackup.

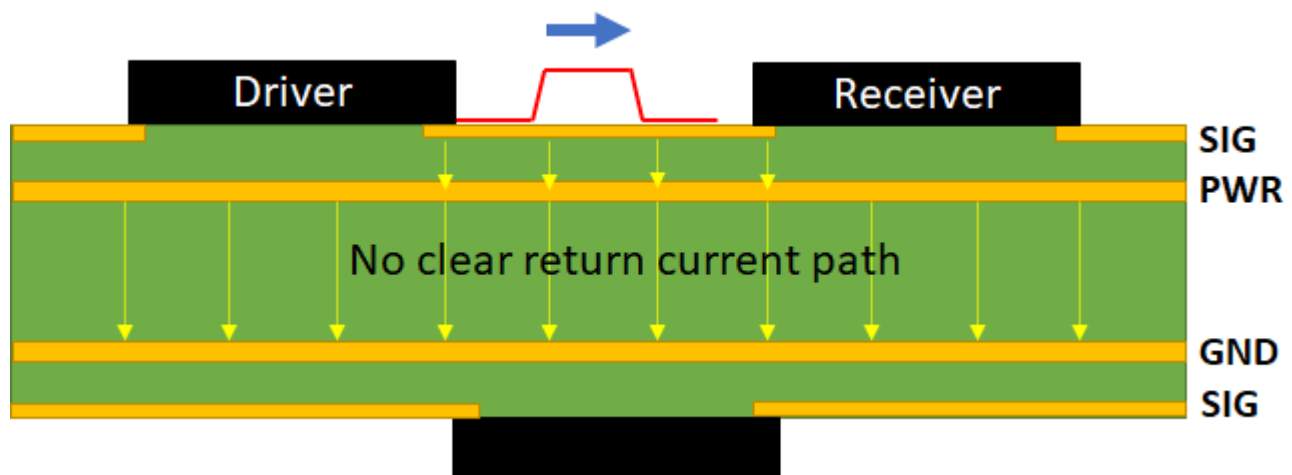
## Why These Stackups Are Better For Single-Ended High Speed Signals

The standard SIG/PWR/GND/SIG stackup for a 4-layer board is still okay for high speed, but you can only reliably support moderate to high speed digital on one side of the board. This is due to the SIG/GND layer pair that is ideal for digital signals; the signal layer that is adjacent to the GND layer is the layer that should be used for digital for the following reasons:

- **Controlled impedance:** The close spacing between the GND layer and the SIG layer allows you to define controlled impedance single-ended traces to 50 Ohms (or some other impedance) without making the traces excessively wide.
- **Shielding:** The SIG+PWR/GND/GND/SIG+PWR stackup will have the highest shielding from internal noise and interlayer crosstalk, while the inverse stackup will have the highest shielding from external noise, but it will have internal crosstalk if not routed correctly.
- **Clear return path:** The capacitively-coupled return path has low impedance because it's being excited directly in the ground plane. Contrast this with the SIG/PWR layer pair, which presents a high impedance return path or a very large return current loop that generates EMI.

The biggest reason you'll see cited for using one of these alternative stackups is the final point in this list, where there is a need to provide a return path. The [return path induced in the power](#)

[plane](#) is unpredictable and could be very large.



*In the SIG/PWR/GND/SIG stackup, it's possible that the digital return current in the PWR plane follows a very large loop back to ground. One path is through the nearest decap, but this does not eliminate low-frequency EMI.*

To try and reduce the loop area and [impedance](#) of the return path for digital signals, one band-aid might be to place some [copper pour on the surface layer around your traces](#) above the power plane. However, the capacitive coupling between the trace and signal could be weak and there is no guarantee of a large reduction in EMI.

Although you only have one ideal layer for digital signals rather than two layers, the standard SIG/PWR/GND/SIG stackup has other merits. With a dedicated power plane, you can still route higher current than you could in copper pour used for routing power; this would be useful in a power system that requires some digital control circuitry. The back layer can be used to hold a variety of other components like connectors or passives.

The important takeaway in the standard 4-layer stackup design, particularly in regards to placing power in a 4-layer board, is this: including a dedicated power layer will not cause your design to automatically fail EMC testing. However, don't assume you can route your digital signals however you want just because you are routing over a uniform power plane. It's more important to understand how a return path propagates in a power plane and how it eventually couples back to ground through a high impedance return path.

No matter what kind of 4-layer PCB stackup you want to build, the easy-to-use design tools in [Altium](#) can help you quickly customize your stackup and create your PCB layout. All users can create schematics, PCB layouts, and manufacturing documentation needed to move a design from idea to production. Users also have access to a personal workspace on Altium, where they can upload and store design data in the cloud, and easily view projects via a web browser in a secure platform.